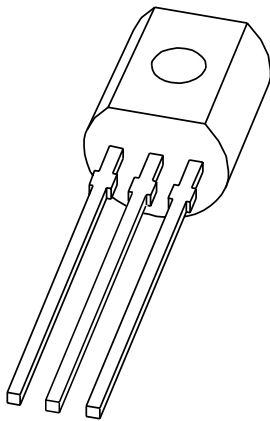


# DATA SHEET



## **BS108**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
Supersedes data of 1997 Jun 17

2001 May 18

# N-channel enhancement mode vertical D-MOS transistor

**BS108**

## FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

## APPLICATIONS

- Line current interruptor in telephone sets
- Applications in relay, high-speed and line transformer drivers.

## DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) package.

## PINNING - SOT54

PIN	DESCRIPTION
1	source
2	gate
3	drain

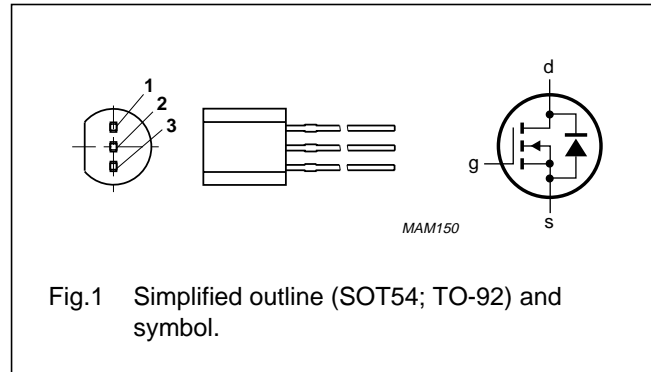


Fig.1 Simplified outline (SOT54; TO-92) and symbol.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)	200	V
$V_{GSth}$	gate-source threshold voltage	1.8	V
$I_D$	drain current (DC)	300	mA
$R_{DSon}$	drain-source on-state resistance	5	$\Omega$

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	200	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	300	mA
$I_{DM}$	peak drain current		–	1.2	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$ ; note 1	–	1	W
$T_{stg}$	storage temperature		–55	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

## Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 × 10 mm.

## N-channel enhancement mode vertical D-MOS transistor

BS108

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	125	K/W

#### Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum  $10 \times 10$  mm.

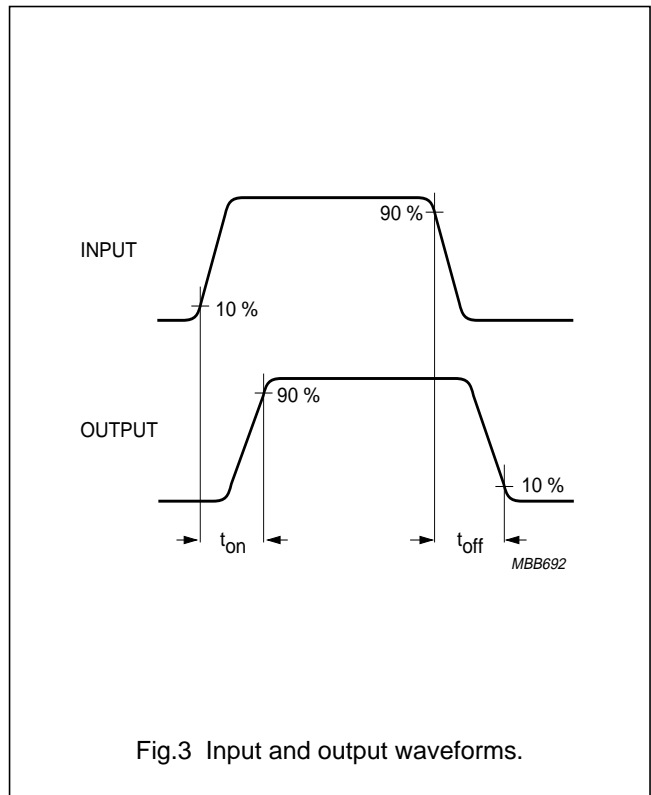
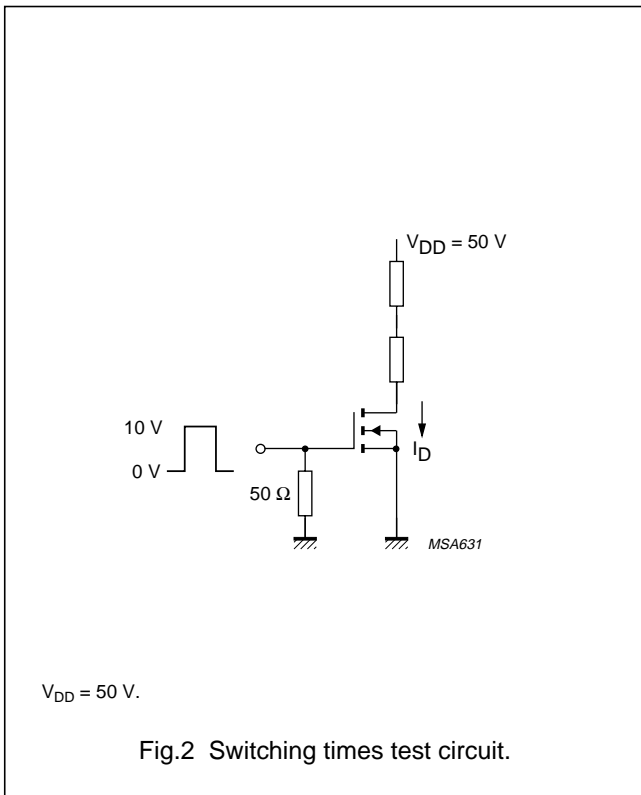
### CHARACTERISTICS

$T_j = 25$  °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu A$ ; $V_{GS} = 0$	200	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 160$ V; $V_{GS} = 0$	–	–	1	$\mu A$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$	–	–	$\pm 100$	nA
$V_{GSth}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{GS} = V_{DS}$	0.4	–	1.8	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 100$ mA; $V_{GS} = 2.8$ V	–	2.7	5	$\Omega$
$ Y_{fs} $	transfer admittance	$I_D = 300$ mA; $V_{DS} = 25$ V	200	600	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$ ; $f = 1$ MHz	–	100	120	pF
$C_{oss}$	output capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$ ; $f = 1$ MHz	–	20	30	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$ ; $f = 1$ MHz	–	10	15	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 0$ to 10 V	–	6	10	ns
$t_{off}$	turn-off time	$I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 0$ to 10 V	–	49	60	ns

# N-channel enhancement mode vertical D-MOS transistor

BS108



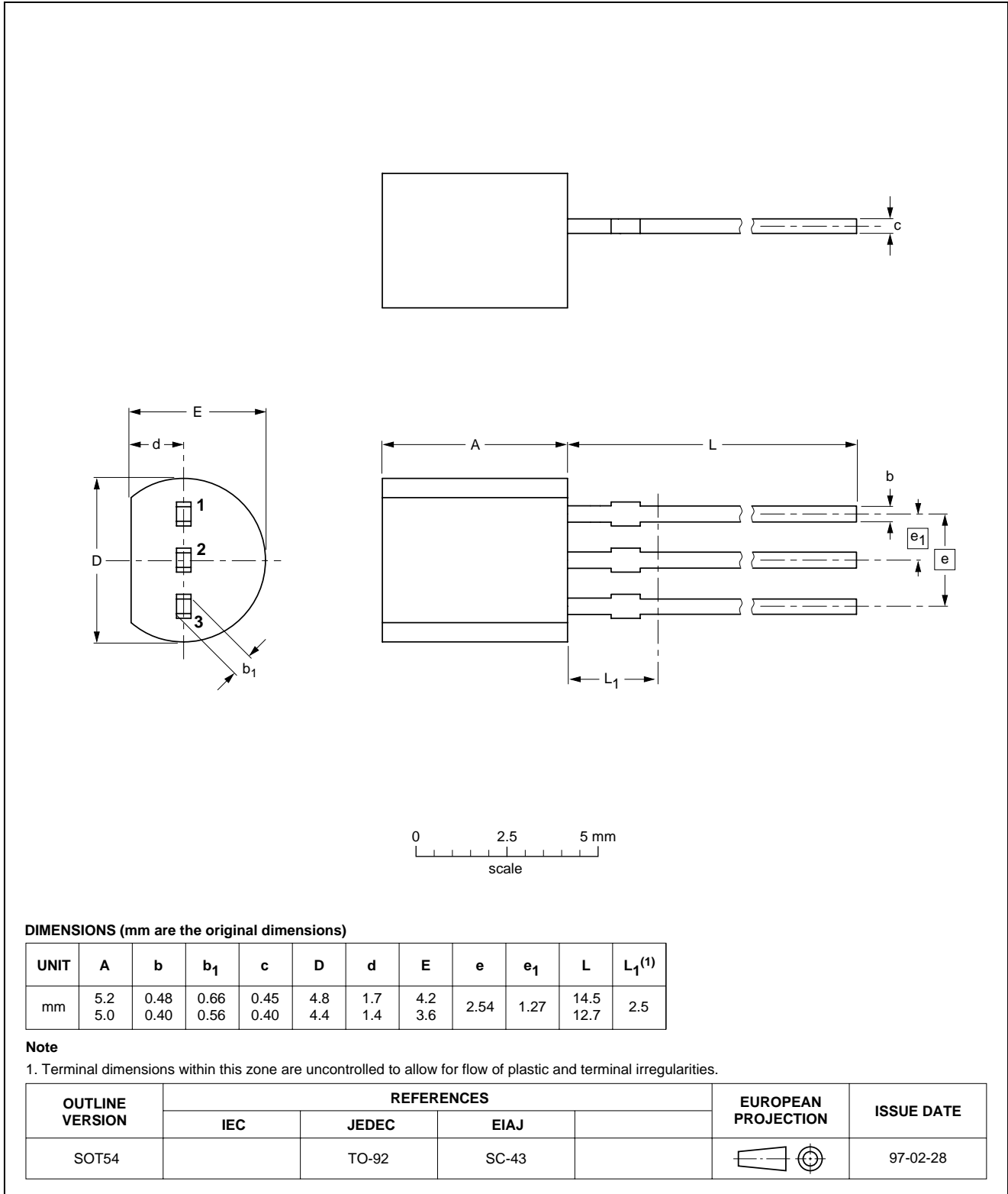
N-channel enhancement mode  
vertical D-MOS transistor

BS108

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



# N-channel enhancement mode vertical D-MOS transistor

BS108

## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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N-channel enhancement mode  
vertical D-MOS transistor

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BS108

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